UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/892,997	06/28/2001	Sin Ho Kang	8733.484.00	6417

30827 7590 02/21/2007 MCKENNA LONG & ALDRIDGE LLP 1900 K STREET, NW WASHINGTON, DC 20006	**EXAMINER** DHARIA, PRABODH M

ART UNIT	PAPER NUMBER
2629	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	02/21/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)
	09/892,997	KANG ET AL.
	Examiner	Art Unit
	Prabodh M. Dharia	2629

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE _3_ MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
  Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on _20 December 2006_.

2a)☐ This action is **FINAL**.   2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under _Ex parte Quayle_, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) _1-8,13-17,21,25-27,29,30 and 32-39_ is/are pending in the application.

     4a) Of the above claim(s) _9-12,18-20,22-24,28 and 31_ is/are withdrawn from consideration.

5)☒ Claim(s) _36-39_ is/are allowed.

6)☒ Claim(s) _1-8,13-17,21,25-27,29,30 and 32-35_ is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on _28 June 2001_ is/are: a)☒ accepted or b)☐ objected to by the Examiner.

     Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

     Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

     a)☒ All   b)☐ Some *   c)☐ None of:

       1.☒ Certified copies of the priority documents have been received.

       2.☐ Certified copies of the priority documents have been received in Application No. _____.

       3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

     * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1)☒ Notice of References Cited (PTO-892)

2)☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3)☐ Information Disclosure Statement(s) (PTO/SB/08)
     Paper No(s)/Mail Date _____.

4)☐ Interview Summary (PTO-413)
     Paper No(s)/Mail Date. _____.

5)☐ Notice of Informal Patent Application

6)☐ Other: _____.

1.   **Status:** Please all the replies and correspondence should be addressed to Examiner's new

art unit 2629. Receipt is acknowledged of papers submitted on 12-20-2006 under request for

reconsideration, which have been placed of record in the file. Claims 1-8, 13-17, 21, 25-27, 29,

30 and 32-39 are pending in this action. Claims 9-12, 18-20, 22-24, 28 and 31 are cancelled.

Claim Rejections - 35 USC § 103

2.   The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all

obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in
> section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are
> such that the subject matter as a whole would have been obvious at the time the invention was made to a person
> having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the
> manner in which the invention was made.

3.   Claims **1, 4-6, 13-17, 21,25-27,29,30,32-35** are rejected under 35 U.S.C. 103(a) as being

unpatentable over Tone (U.S. Patent 6,046,712) in view of Margulis et al. (6,157,396) and

Nishimura et al. (6,169,505 B1).

Regarding **independent claims 1, 13, 21, 29, and 34** Tone teaches an apparatus for providing a

gamma voltage correcting apparatus for a liquid crystal display (column 17, lines 60-62; column 59-67,

figure 17 at 615a) wherein video data is corrected by a preset gamma voltage to display an image

entering desired values for the x- and y-coordinate data X_n and Y_n to facilitate the operation of gamma

correction (column 14, lines 1-15, figure 16-19 at 615).

Furthermore, Tone teaches how the apparatus comprises a memory means by external data RAM 403

for storing gamma correction for controlling the gamma voltage for each of at least two modes by

teaching how the data entry unit 615 enters data to the external data RAM 403 via the external CPU,

which activates the mode change signal and the grayscale level such that users can use the data entry

unit 615 to write gamma correction data in the external RAM 403 (column 13, lines 28-44, figure 15 at 403, 615).

Also, Tone teaches a control means by teaching CPU 513 which activates the mode change signal and the grayscale level such that users can use the data entry unit 615 to write gamma correction data in the external RAM 403 (column 13, lines 28-44, figure 15 at 403, 615).

Furthermore, Tone teaches a multi-channel gamma voltage generator for responding to the gamma data for a mode selected by the control means to generate n gamma voltages (wherein n is an integer) having a different voltage level indicated by the gamma data for the selected mode by teaching a gamma correction device 400 with external RAM 403 that includes a plurality of grayscale level correction groups wherein each of the grayscale level data sets has a different number n which is the number for dividing the grayscale level range (column 12, lines 10-36, figure 13 at 300, 400).

However, Tone fails to recite or disclose video data modulated by a gamma voltage correction apparatus are applied r to the data lines of a display device, via a column driver; on the other hand Margulis et al. discloses video data modulated by a gamma voltage correction apparatus are applied to the data lines of a display device, via a column driver (Col. 13, Lines 35-47, Line 62 to Col. 14, Line 5, Col. 16, Line 33 to Col. 17, Line 65, Col. 18, Lines 8-26, Col. 19, Line 36 to Col. 20 Line 23, Col. 24, lines 17-23) and Margulis et al. teaches receiving video data (Col. 6, Lines 53-61 receiving industry standard (NTSC, PAL, S-Video) video data) and vertical and horizontal synchronizing signals and outputting the video data and a clock (Col. 7, Lines 4-12, Lines 26-38, Col.9, Lines 1-5 receives composite data has horizontal and vertical timing component and sampling of video data (clocking) occurs at 100 MHZ). It is well known to a person of ordinary skill in the art, the composite video data such as NTSC, PAL or S-video carries not only video data but also Horizontal, vertical, and clocking information (see Taubman et al. (6,297,851 B1) Col. 1, Lines 11-32, Col. 7, line 53 to Col. 8, Line 13).

Thus, it would have been obvious to a person of ordinary skill in the art to combine Tone and

Margulis et al. because while Tone teaches how a CPU 513 activates a <u>mode change signal</u> and the

<u>grayscale level</u> such that users can use the data entry unit 615 <u>to write gamma correction data</u> in the

external RAM 403 (column 13, lines 28-44, figure 15 at 403, 615), Margulis et al. teaches how the

LCD (Col. 6, Line 37) comprises a column driver for correcting the video data by performing <u>gamma</u>

<u>correction</u> and supplying the corrected video data to the data lines (Col. 13, Lines 35-47, Line 62 to

Col. 14, Line 5, Col. 16, Line 33 to Col. 17, Line 65, Col. 18, Lines 8-26Col. 19, Line 36 to Col. 20

Line 23, Col. 24, lines 17-23). The motivation for combining these inventions would have been to

provide optimized a high quality display device (Col. 1, Lines 8-11).

Tone fails to recite or disclose a multi-channel gamma voltage generator having a plurality of

digital to analog converters (DACs), the digital to analog converters generating n gamma voltages

(wherein n is an integer) having a different voltage level in response to the digital gamma data

respectively. However, Nishimura et al. discloses a multi-channel gamma voltage generator having a

plurality of digital to analog converters (DACs) (Col. 4, Lines 45-56, Col. 11, Lines 12-35), the digital

to analog converters generating n gamma voltages (wherein n is an integer) having a different voltage

level in response to the digital gamma data respectively (Col. 4, Lines 45-56, Col. 11, Lines 12-35,

please see figures 2-6).

Thus, it would have been obvious to a person of ordinary skill in the art to combine Tone and

Nishimura et al. because while Tone teaches how a CPU 513 activates a <u>mode change signal</u> and the

<u>grayscale level</u> such that users can use the data entry unit 615 <u>to write gamma correction data</u> in the

external RAM 403 (column 13, lines 28-44, figure 15 at 403, 615), Nishimura et al. teaches the LCD

(Col. 1, Lines 42-45) comprises a multi-channel gamma voltage generator having a plurality of digital

to analog converters (DACs) (Col. 4, Lines 45-56, Col. 11, Lines 12-35, please see figures 2-6).), the

digital to analog converters generating n gamma voltages (wherein n is an integer) having a different

voltage level in response to the digital gamma data respectively (Col. 4, Lines 45-56, Col. 11, Lines 12-35, please see figures 2-6). The motivation for combining these inventions would have been to provide the single time-varying analog signal derived from the single digital sequence at an operational speed at which high accuracy and low power consumption can be easily attained enables well-matched digital-to-analog conversions to be performed in any number of channels ranging from a few to many thousands. (Abstract).

Regarding **claims** 4 and **5,** in further discussion of claim 1, Tone teaches how gamma data for the selected mode by teaching a gamma correction device 400 with external RAM 403 that includes a plurality of grayscale level correction groups wherein each of the grayscale level data sets has a different number n which is the number for dividing the grayscale level range (column 12, lines 10-36, figure 13 at 300, 400).

Regarding **claim 6,** in further discussion of claim 1, Tone teaches how the memory means and the control means are integrated into a single integrated circuit (figure 13 at 400, 312, 403).

Regarding **claims 2, 14-17, 25-27, 30, 32, 33 and 35** in further discussion of claims 13, 21, 29, and 34 Tone teaches a gamma correction device 400 with external RAM 403 that includes a plurality of grayscale level correction groups wherein each of the grayscale level data sets has a different number n which is the number for dividing the grayscale level range (column 12, lines 10-36, figure 13 at 300, 400).

Margulis et al. discloses video data modulated by a gamma voltage correction apparatus are applied r to the data lines of a display device, via a column driver and user controlled (Col. 13, Lines

35-47, Line 62 to Col. 14, Line 5, Col. 16, Line 33 to Col. 17, Line 65, Col. 18, Lines 8-26Col. 19, Line

36 to Col. 20 Line 23, Col. 24, lines 17-23, Col. 24, lines 31-39, Col. 5, Lines 54-58).

4.   **Claims** 3, 7 and **8** are rejected under 35 U.S.C. 103(a) as being unpatentable over *Tone (U.S.*

Patent 6,404,512) in view of Margulis et al. (6,157,396) as applied to claims **1, 4-6, 13-17, 21,25-**

27,29,30,32-35 above and further in view of *Hiroki (U.S.* 6,771,238).

Regarding claims **3,** in further discussion of claim 1, Tone modified by Margulis et al. teaches

a gamma correcting apparatus for a liquid crystal display (column 14, lines 1-15, figure 16-19 at 615).

However, Tone modified by Margulis et al. does not teach how the LCD comprises a column

driver for correcting the video data using the gamma voltage from the multi-channel gamma voltage

generator and supplying the corrected video data to the data lines. On the other hand, Hiroki discloses

an active matrix display device, comprising a plurality of pixels arranged in a matrix form a first driver

circuit connected to scanning lines and a second driver circuit connected to signal lines (column 4, lines

29-35) wherein the video signal processing circuit 20 mainly performs gamma correction such that the

processed video signal is inputted from the source driver circuit 13 through the signal line 18 to the

pixel matrix area 11, thus applied to the pixel electrode of the liquid crystal cell 15 (see column 1, lines

66 through column 2, lines 1-15).

Thus, it would have been obvious to a person of ordinary skill in the art to combine Tone

modified by Margulis et al. and Hiroki because while Tone teaches how a CPU 513 activates a mode

change signal and the grayscale level such that users can use the data entry unit 615 to write gamma

correction data in the external RAM 403 (column 13, lines 28-44, figure 15 at 403, 615) and Margulis

et al. discloses video data modulated by a gamma voltage correction apparatus are applied r to the data

lines of a display device, via a column driver (Col. 13, Lines 35-47, Line 62 to Col. 14, Line 5, Col. 16,

Line 33 to Col. 17, Line 65, Col. 18, Lines 8-26Col. 19, Line 36 to Col. 20 Line 23, Col. 24, lines 17-

23), Hiroki teaches how the LCD comprises a column driver for correcting the video data by

performing gamma correction and supplying the corrected video data to the data lines (see column 1,

lines 66 through column 2, lines 1-15). The motivation for combining these inventions would have

been to provide a high quality display device (column 3, lines 15-21).

Regarding **claims** 7 and **8,** in further discussion of claim 3, Hiroki discloses an active matrix

display device, comprising a plurality of pixels arranged in a matrix form a first driver circuit

connected to scanning lines (column 4, lines 29-35) wherein a timing controller via the video

processing circuit 110 facilitates the supply of red, green and blue digital video data to the column

driver and for applying a desired timing control signal to the row driver (see column 5, lines 32-62).

Allowable Subject Matter

5.   Claims 36-39 are allowed.

6.   The following is an examiner's statement of reasons for allowance: The claim 36 was

allowed in non-final office action mailed on 11-29-2005, the newly added claims 37-39 depend

from independent claim36, therefore after further search and consideration claims 37-39 are also

allowable.

A display device having a gamma voltage correcting part, wherein the display device has

a display panel that includes a plurality of pixels defined by gate lines and data lines, the display

device comprising: a display controller for receiving a first video data and vertical and horizontal

synchronizing signals and outputting a second video data and a clock; **a lookup table driver**

connected to the display controller for adjusting color temperature of the second video data

and outputting a third video data; the gamma voltage correction part including', a memory

for storing at least two sets of gamma data for at least two input modes, a gamma

controller for accessing one set of the gamma data in response to a selection signal, a multi-

channel gamma voltage generator for responding to the one set of the gamma data to

generate n gamma voltages (wherein n is an integer) having different voltage levels, and a

column driver connected to the display panel, wherein the column driver receives the third

video data and the n gamma voltages, and then corrects the third video data using the n

gamma voltages and applies the corrected video data to the data lines.

The cited references fails to disclose above underlined bold claim.

Any comments considered necessary by applicant must be submitted no later than the

payment of the issue fee and, to avoid processing delays, should preferably accompany the issue

fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for

Allowance."

Response to Arguments

7.   Applicant's arguments, see remark, filed 12-20-2006, with respect to the rejection(s) of

claim(s) **1, 13, 21, 29, and 34** under traversing and request for reconsideration have been fully

considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon

further consideration, a new ground(s) of rejection is made in view of Nishimura et al.

(6,169,505 B1).

Conclusion

8.   The prior art made of record and not relied upon is considered pertinent to applicant's

disclosure.

Mayer, III; Theodore et al. (US 6115022 A) Method and apparatus for adjusting multiple

projected raster images.

9.   Any inquiry concerning this communication or earlier communications from the

examiner should be directed to Prabodh M. Dharia whose telephone number is 571-272-7668.

The examiner can normally be reached on M-F 8AM to 5PM.

10.   The fax phone number for the organization where this application or proceeding is

assigned is 571-273-8300.

11.   Information regarding the status of an application may be obtained from the Patent

Application Information Retrieval (PAIR) system. Status information for published applications

may be obtained from either Private PAIR or Public PAIR. Status information for unpublished

applications is available through Private PAIR only. For more information about the PAIR

system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR

system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

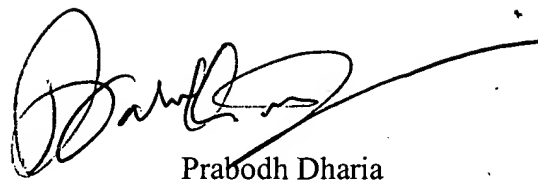Any response to this action should be mailed to:

Commissioner of Patents and Trademarks

Washington, D.C. 20231

Prabodh Dharia

Partial Signatory Authority

AU 2629

February 15, 2007